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| Digital Simulation Using Verilog in Modelsim  Experiment 9 |
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**DIGITAL LOG****IC DESIGN (CSE1003)**

**Exp#9 – Digital Simulation using ModelSim**

## Objectives:

* To write the Verilog HDL code for various digital circuits.
* Simulate them using the ModelSim Altera Software
* Test them using appropriate test benches.

**Softwares Used:**

* ModelSim Altera 10.1d (Quartus II 13.0sp1)

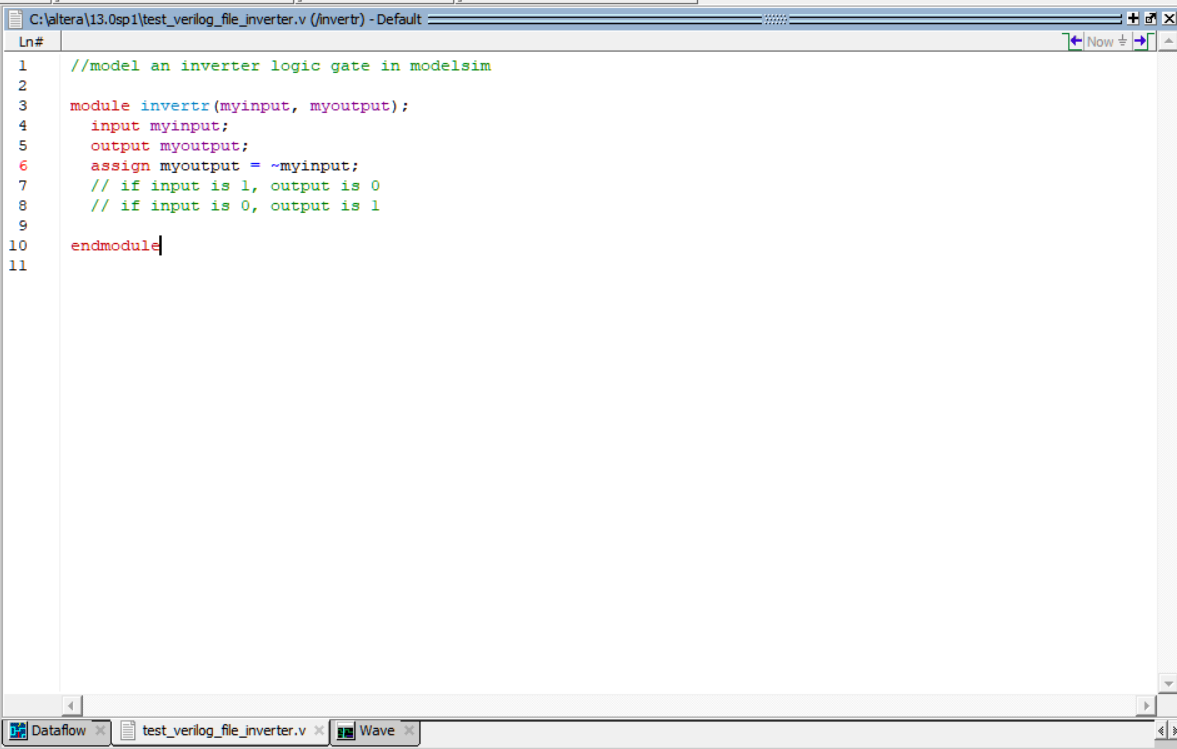
## Theory:

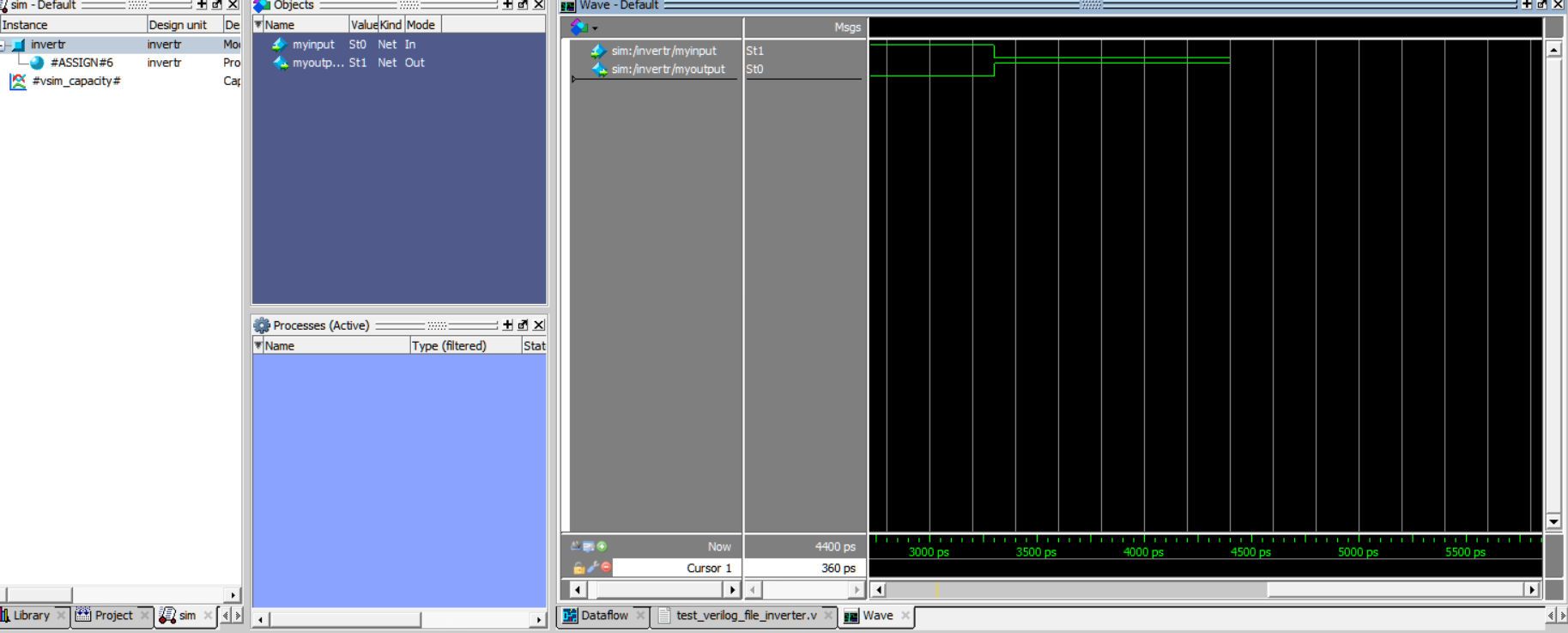
**Verilog** is a hardware description language (HDL) used to model electronic systems. It is most commonly used in the design and verification of digital circuits at the register-transfer level of abstraction. It is also used in the design and verification of analog, digital and mixed-signal circuits.

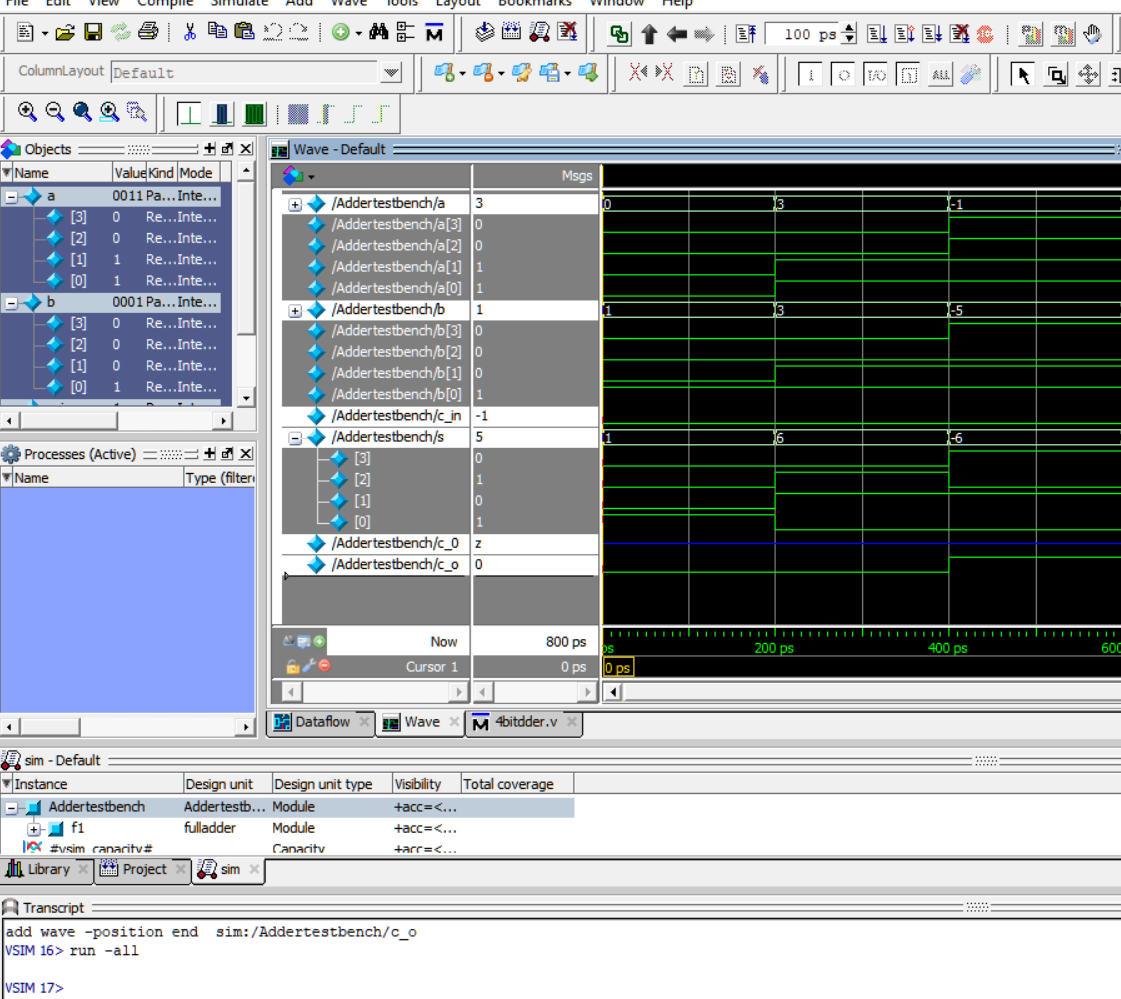
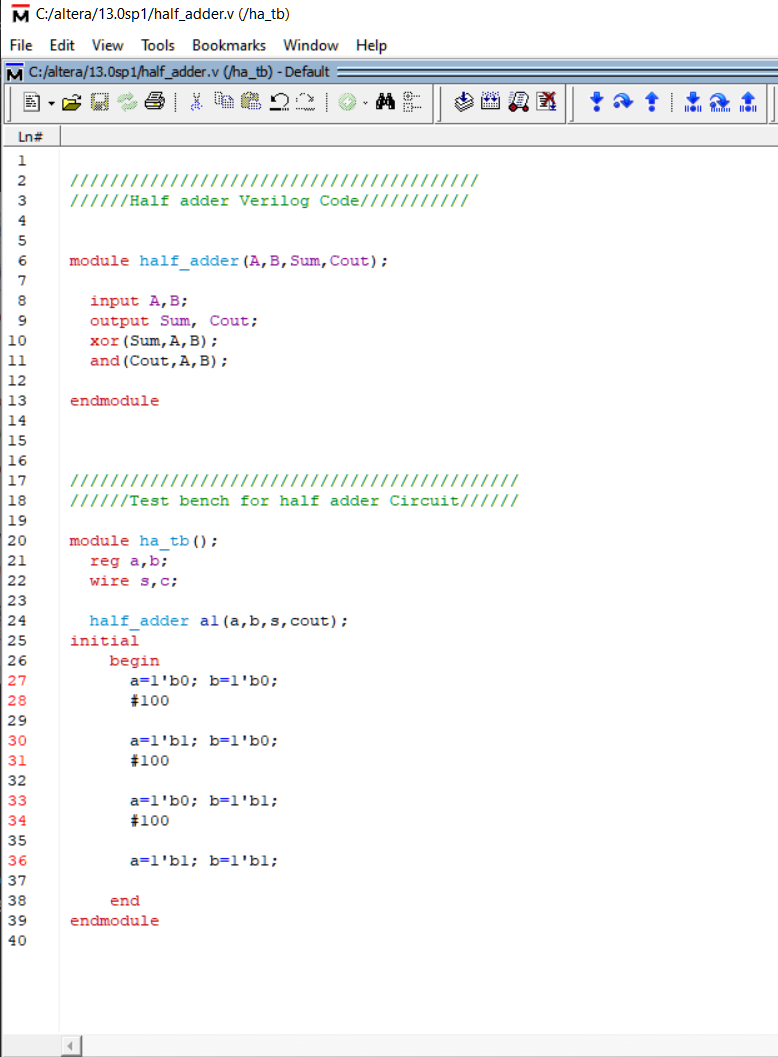
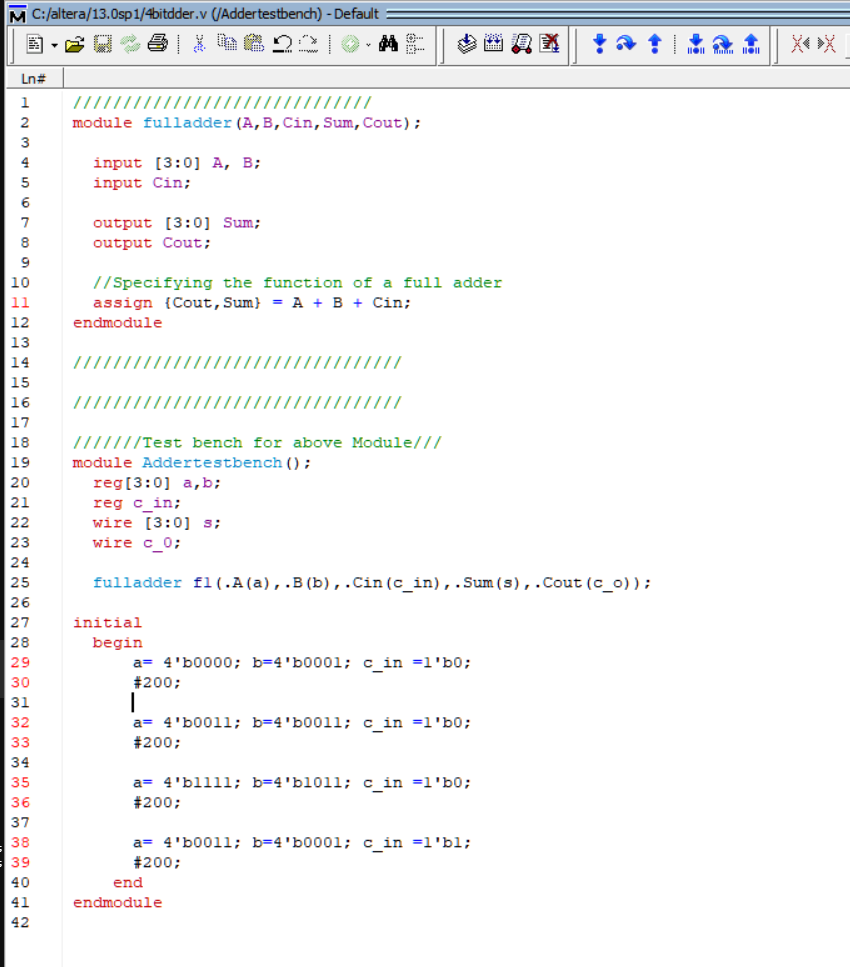
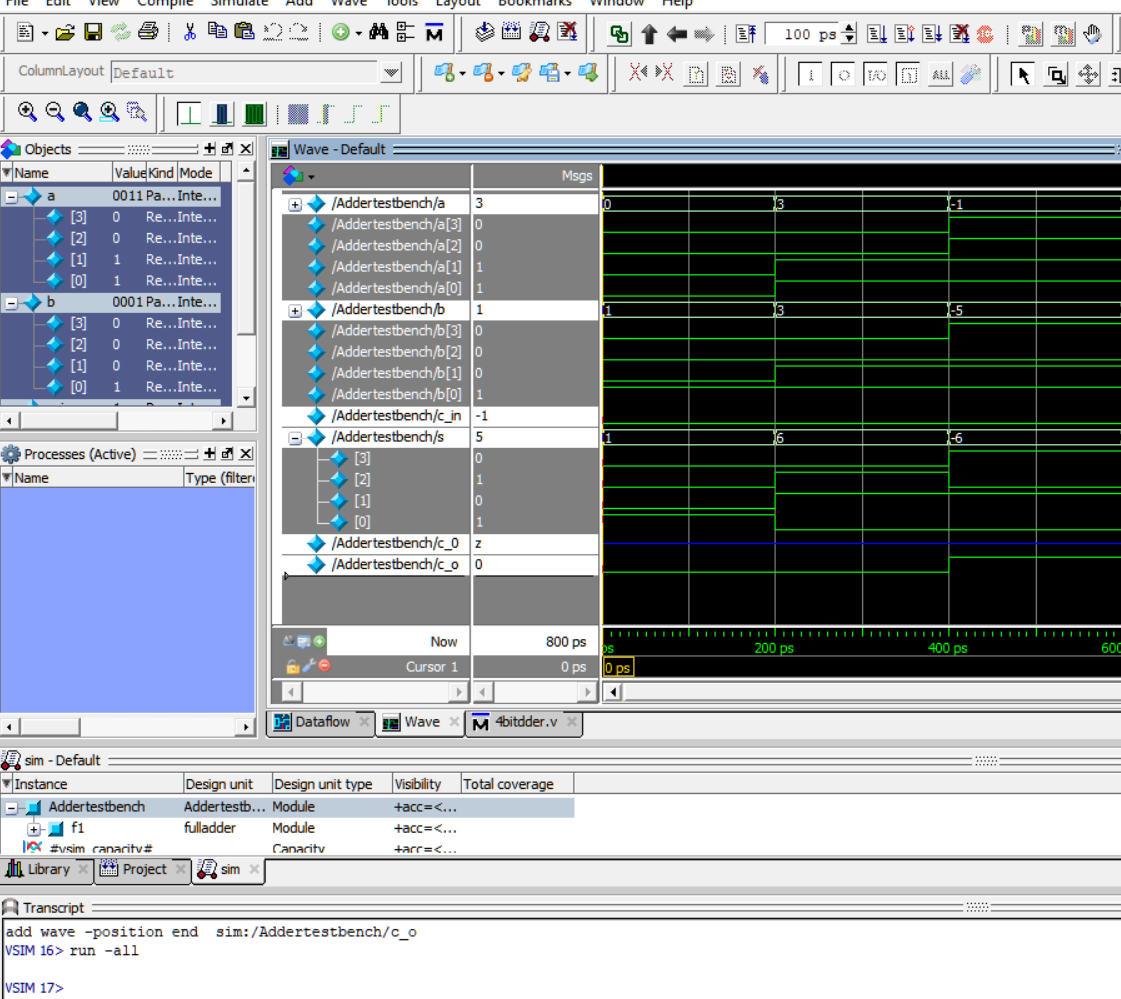
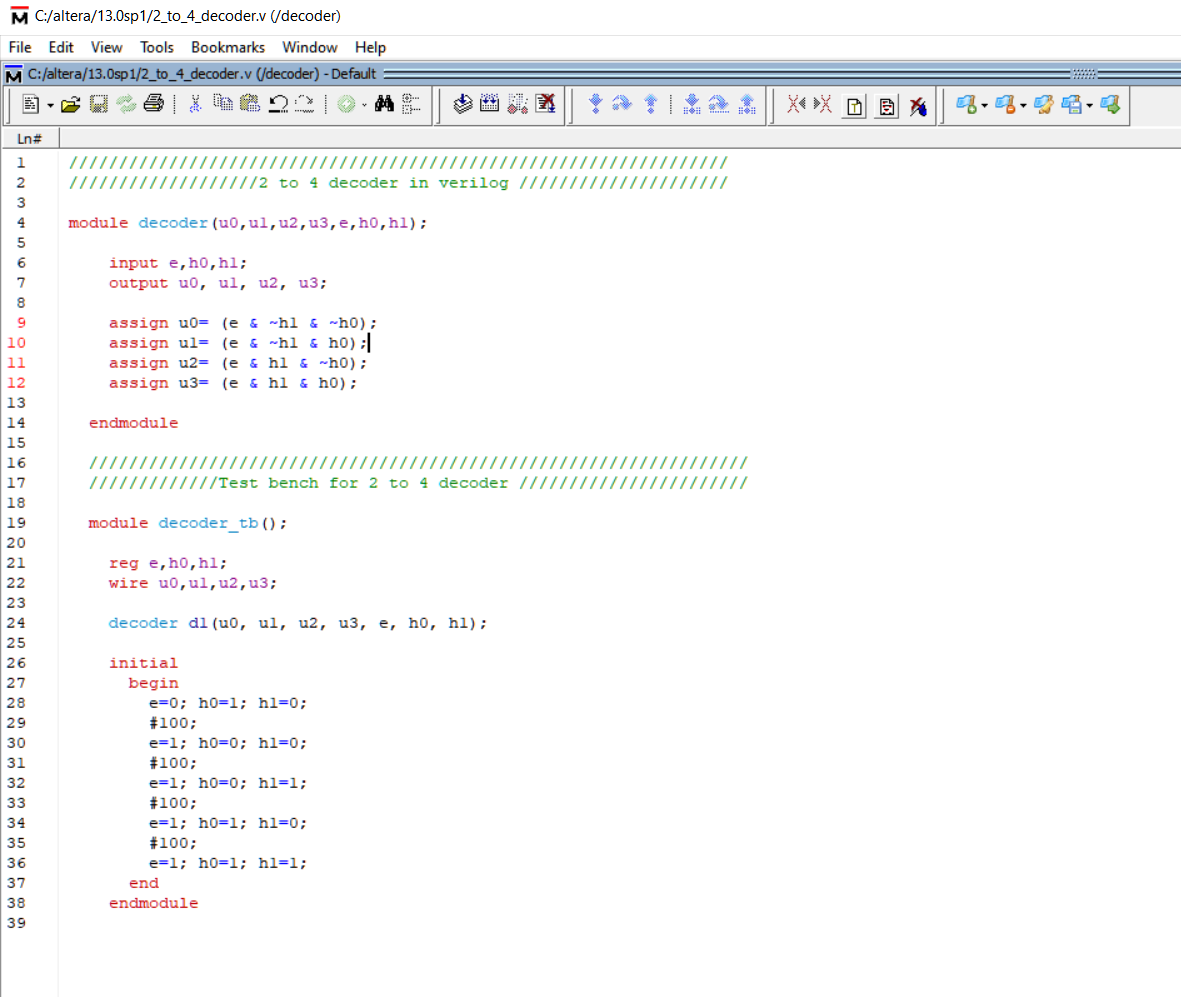
**ModelSim** is a Software environment developed by Mentor Graphics for the simulation of hardware description languages such as VHDL, Verilog, etc.

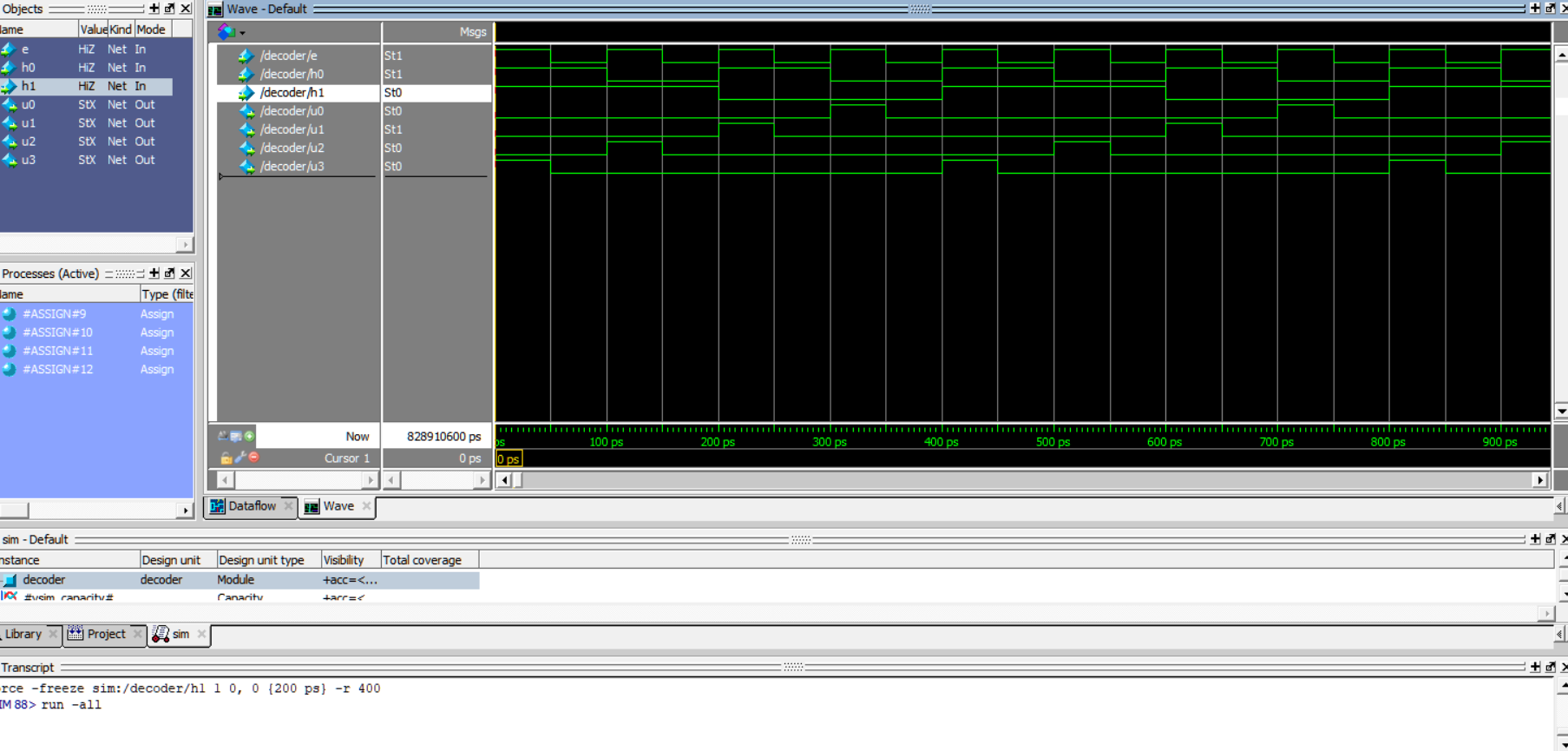
In this experiment, we use ModelSim Software Environment to design, model and test various digital Circuits.

1. Verilog Simulation of a basic Inverter:

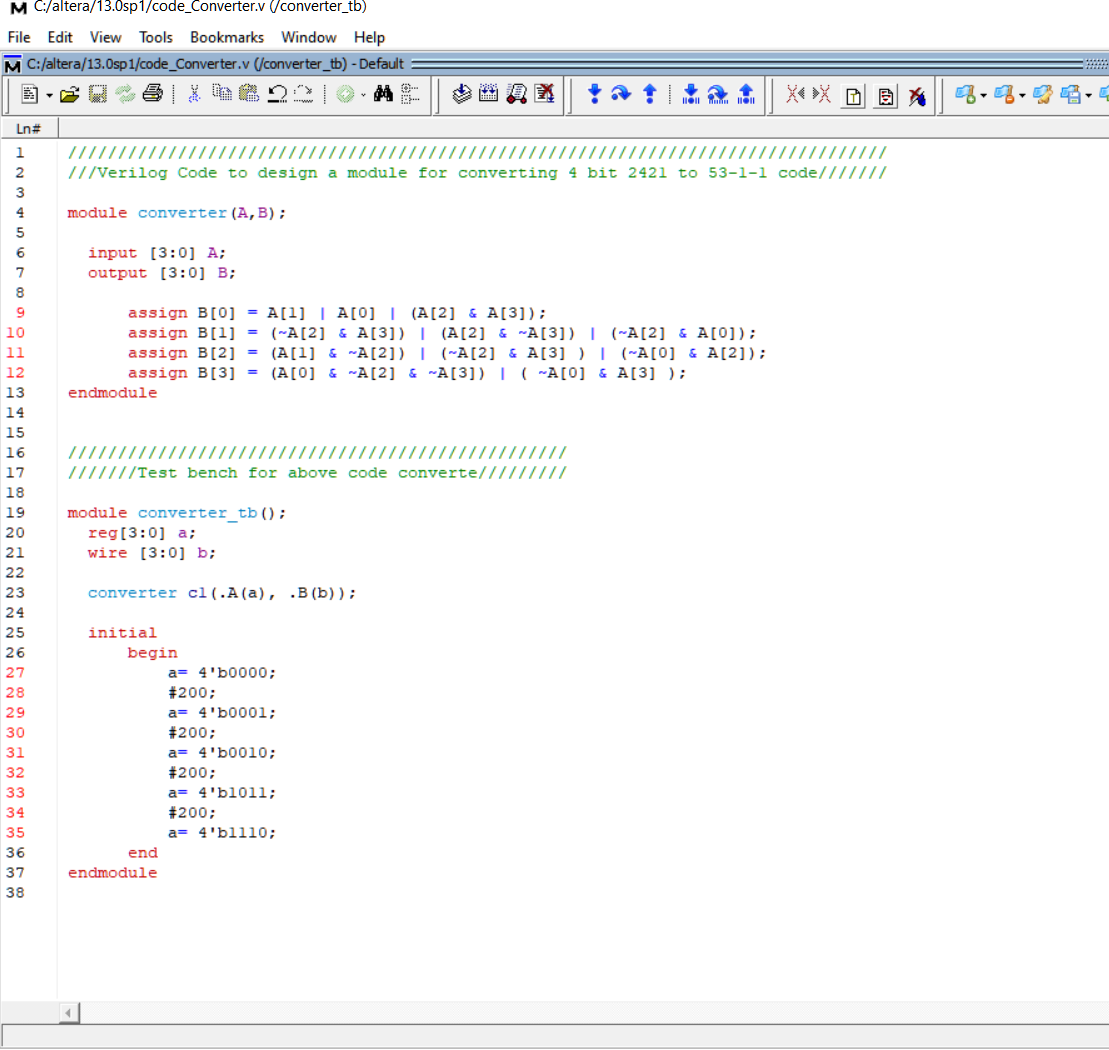


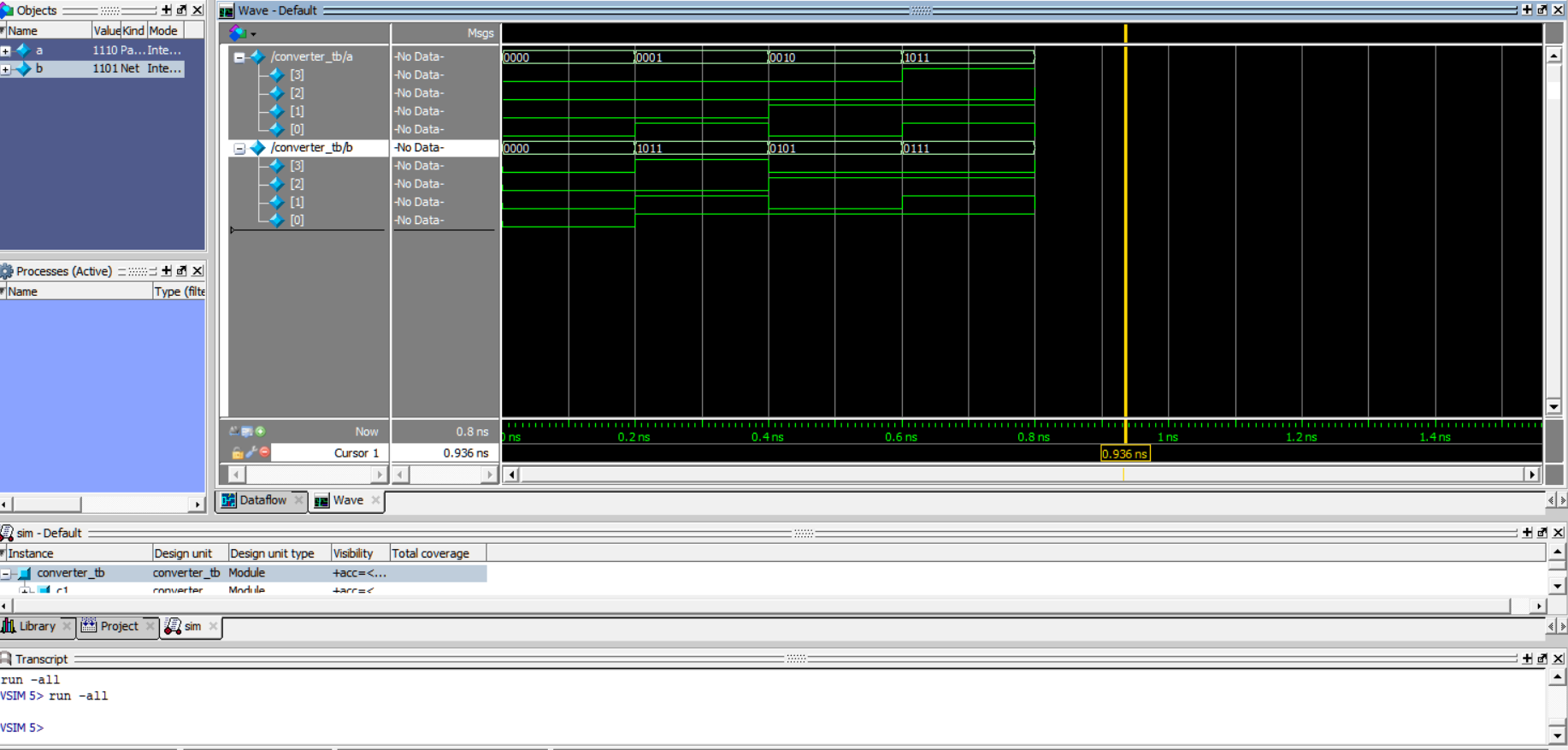


1. Verilog Simulation of a half Adder: 
2. Verilog Simulation of a Full Adder:  
3. Verilog Simulation of a 2 to 4 decoder:



1. **Verilog Simulation of 2421 to 53-1-1 Code Converter (DA2).**





***CONCLUSION/ INFERENCES:***

From the above experiments, we can observe that any digital circuits can be simulated by writing a proper Verilog(HDL) code of the corresponding circuit. HDL compilers like ModelSim help to convert the code into it’s circuit equivalent which can further be tested with a test bench and the design can be further implemented in FPGAs if required.